ML4079D

Technical Reference

400G Bit Error Ratio Tester

Innovation for the next generation

multiLane

Table of Contents

ML4079D | Key Features

- Data Rates in NRZ mode 9 – 15 and 21-30 Gbps.
- Ability to tune the bit rate in steps of 100 kbps and find the RX PLL locking margin.
- Data Rates in PAM4 mode 21 - 30 GBd.
- High frequency clock out > 2.4 GHz
- Independent control of inner eye levels
- Up to 1.5 Vppd output swing
- Supports Gray coding and polarity inversion

Recommended Operating Conditions

Parameter	Notes/Conditions	Max	Units
Operating Temperature	this temperature is considered as the cutoff value	65	°C
Supply Voltage	110/220 adapter used to power-up the board		V

General Description

ML4079D is a fully featured 400G BERT that can be configured as an 8x29.5 GBaud BERT. At high rates both NRZ and PAM4 modes are supported. It is used in Production testing of transceivers as for Functional and SI testing.
The **ML4079D** is designed for 400G applications. This instrument is a fully integrated, ultra-compact, USB/Fast Ethernet controlled instrument that combines all the functions and features of a signal generator, bit error-ratio tester and data analysis system with Post Emphasis and Pre Emphasis and CTLE capabilities.

1. ML4079D Ordering Information

The instrument can be ordered with the following part number.

Part Number	Description
ML4079D	8 channels BERT

For more details please refer to the below link:
https://multilaneinc.com/product/ml4079d/

2. Block Diagram

The ML4079D block diagram is illustrated in figure 1. Signals are transmitted from the TX side through eight independent channels, and the received signals are routed from the RX side of the error detector. These signals can be monitored and controlled channel by channel.

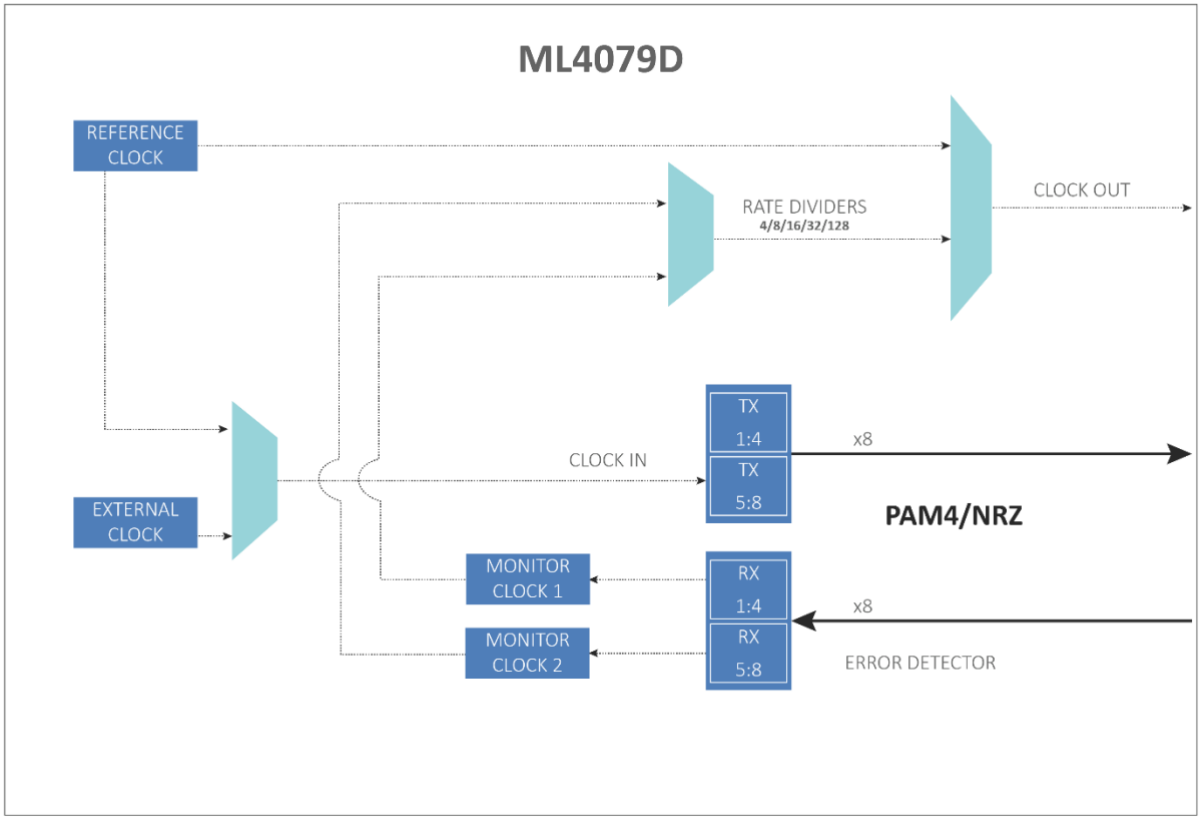


Figure 1: Block Diagram of the ML4079D

3. Hardware design overview

Figure 2 shows a general view of the ML4079D.

Figure 2: ML4079D mechanical drawing

The instrument dimensions in mm are shown in figures 3 and 4.

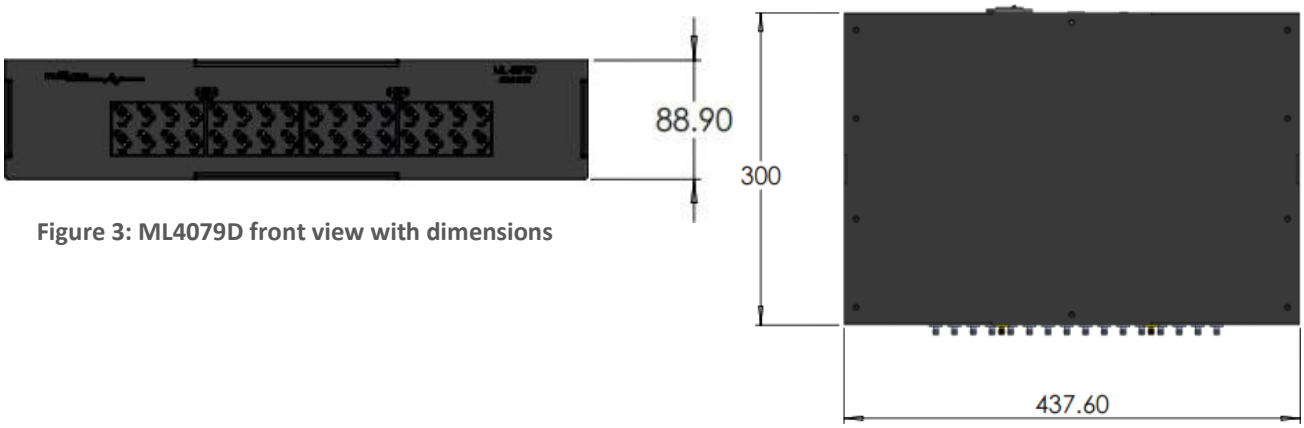


Figure 3: ML4079D front view with dimensions

Figure 4: ML4079D front view with

With an overall weight of four kilograms.
The back plate includes an ON-OFF switch button, Ethernet and USB ports. A 110/220V power adapter can be connected to supply the board with the required power.
The faceplate shows two SMA connectors for clock connection: clock-in and clock-out.

Also the faceplate shows thirty-two connectors type K (2.92mm connectors) that are used to connect to the eight differential TX and RX channels. Once powered up, and the switch button turned on, the board should be able to perform all the required measurements.

4. Clock Configuration

The ML4079D supports input and output clocks.

For the Clock out: The user can switch between two options the reference clock and monitor clock. The monitor clock supports the following rate dividers: 8, 16, 32, 64, and 128.
The reference clock has an optimal value of 156.25 MHz.

The analog clock input range varies between 136.36 -178.78 MHz with an optimal value of 156.25MHz.

5. Transmitter Side Characteristics

As described above the TX signals are transmitted through eight independent channels.
The optimal settings for each channel, generated during the calibration process, at scaling 70 and 80%, are being applied at high and low rates, and in both eye modes: NRZ and PAM4 (PAM4 only supported at high rate).
These settings, once applied and saved, during calibration, ensure that the ML4079D performs all the required measurements.

These settings can be controlled by the user in advanced mode, in this way the user can control all the TX settings including: TX pattern, amplitude, Pre-emphasis, Main-Tap, Post-Emphasis or the 7 FIR taps…

The ML4079D operates in PAM4 and NRZ modes, on numerous bitrates.
The BERT locks on all the supported rates, amplitudes and patterns. The parameters are mentioned in table 2.
The TX Equalization is a digital combination of FFE and DFE. PAM4 gray coding is also supported. Test pattern generator per lane includes error injection.
The patterns, error insertion and emphasis taps can be checked and controlled per lane. The user has the ability to turn off and disable the TX side channel by channel.

Kindly refer to the user manual paragraph 11 for more details on how to operate the ML4079D.

The table below shows the TX Output Characteristics of the ML4079D.

Parameter			Typical	Maximum	Unit
Line Rate	NRZ		9 - 14.2 22 - 29.5	up to 29.5	Gbps
	PAM4		22 - 29.5	up to 29.5	Gbaud
Clock-out Amplitude			TBD		mV
Clock-in Amplitude			400 -1600		mVpp
Clock-out Frequency	Monitor		Rate dividers: 8, 16, 32, 64, 128	Up to Rate/8	MHz
	Reference		156.25	136.36 -178.78	
Output Amplitude	Low Rate (NRZ)	Advanced Mode	Up to 1200		mV
		70% Calibrated	Up to 900		
		80% Calibrated	Up to 1150		
	High Rate (NRZ & PAM*4)	Advanced Mode	Up to 1200		
		70% Calibrated	Up to 830		
		80% Calibrated	Up to 1000		
Patterns			PRBS 7/9/11/13/15/16/23/31 PN9_4, PNJP083B, LIN, CJT, SSPRQ, User Defined		
Transition time (20%-80%)	Low Rate		>14		ps
Transition time (20-80%)	High Rate		>18.5		
Jitter	Low Rate		TBD		ps
	High Rate		TBD		

6. Receiver Side Characteristics

The receiver side characteristics are described in this section.
The BERT locks on different patterns, with the polarity inversion option. The equalizer can be tuned on a range of around 8 dB. A FEC emulator is supported on this board, which is a monitor located after the PRBS verifier that analyzes the RX errors to estimate the FEC errors that would have been achieved if the link had been FEC encoded. There is not a FEC encoder at all the TX channels and the RX cannot lock to a FEC encoded pattern. Real-Time BER can be measured. Histograms and SNR shared across all eight channels. Octal port CDR, being able to recover the supported rates.

Parameter		Typical	Maximum	Unit
Line Rate	NRZ	9 - 14.2 22 - 29.5	up to 29.5	Gbps
	PAM4	22 - 29.5	up to 29.5	Gbaud
Clock-in Amplitude		400 -1600		mVpp
Clock-in Frequency		156.25	136.36 -178.78	MHz
Sensitivity	Low Rate	80		mV
Sensitivity	High Rate	100		
Patterns		PRBS 7/9/11/13/15/23/31		
CTLE			64	Steps

7. Current Revisions

The current revision of the ML4079D hardware is: ML4079D Rev A
All the listed features are tested using the following software and firmware:

- Software revision: Setup MLBert- v4.1.r8050
- Firmware revision: 1.8

8. Future Features

The following feature will be implemented in the future ML4079D versions:

- Calibrated CTLE slider

9. User Manual

9.1. GUI General Description

This section describes how to operate the ML4079D and all the capabilities of this BERT. The product software is available on the company's website on the below link:

https://multilaneinc.com/berts-gui/

9.2. Installation

This chapter covers the installation of the instrument, addressing the following topics:

- System Start-up
- How to connect to the instrument

Note: For windows vista, 7, 8 and 10 users should always run the GUI as administrator.

First Steps

When the customer receives the instrument, it has a pre-configured IP address from the factory. This IP address is printed on a label on the instrument's backplate. The user can choose to keep this IP or to change it. If changing the IP is needed, there are two ways to do it: either through the USB interface, or through the Ethernet interface. If changing through USB is selected, then the USB driver of this instrument should be installed from the company's website, and the user needs to choose the application ETH config.
If the LAN interface is used to change the IP, then the user has to download the application "IPChanger" from the company's website and temporarily change his PC's IP to be in the same domain as the instrument, i.e. 172.16.xx.xx. Once the instrument's IP is successfully changed, the user can change back his PC's IP.

- It would be good if the user prints a label with the newly assigned IP address and sticks it on the instrument. If for some reason the IP is lost, the user will need to use the USB interface together with the ETHconfig software to "read" the IP.

Connect through Ethernet:

In order to connect via Ethernet, the IP address of the board is required. While no drivers are required; the user should simply know the current board IP address, and need to enter it in the text box next to the **IP** label, then click on the **connect** button.
The user can make sure that he is connected, by pinging the device.
To change the IP address of the board, the user needs to install the USB drivers. (Refer to paragraph 12).

After installing the setup, the user will be able to open the ML4079D GUI.

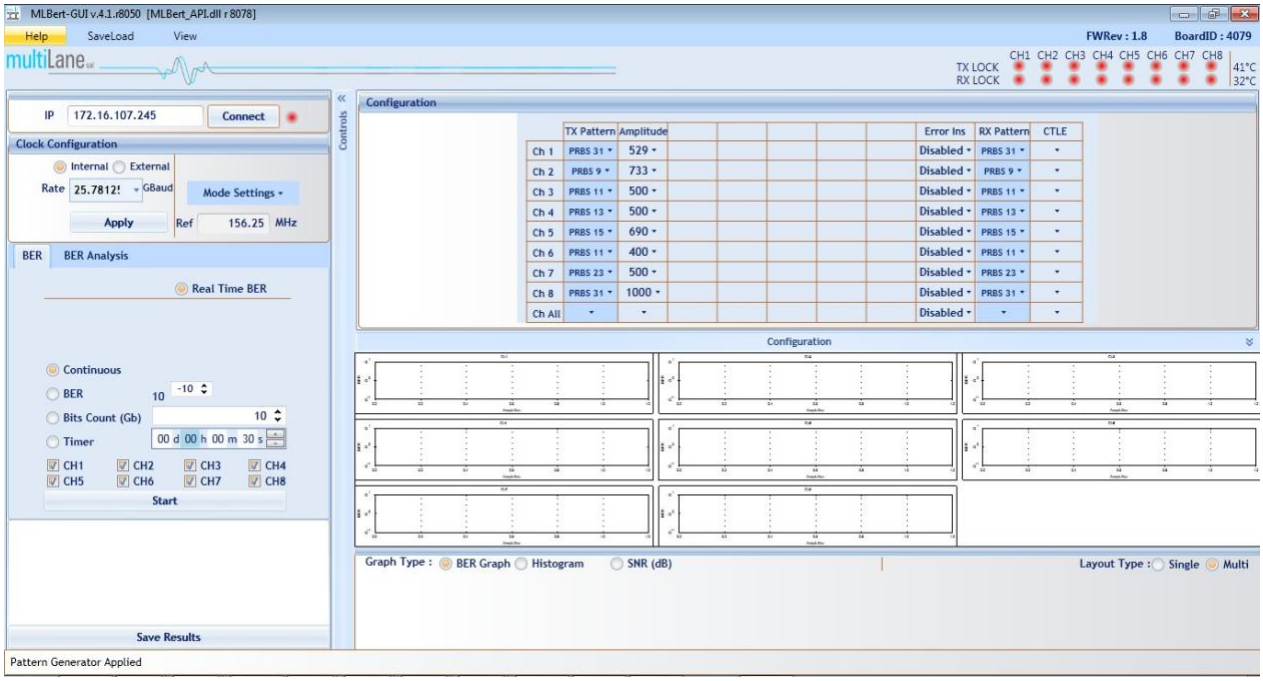


Figure 5: ML4079D GUI

9.3. Connecting Procedure

The user needs to connect using the board's IP, after that the board has been powered-up.

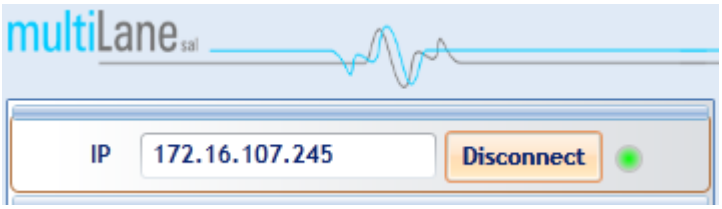


Figure 6: Connecting using the board IP

After clicking on Connect, all the optimal settings that have been saved during the calibration are being applied. Also the last used configuration are being applied.

Then the user can check the board's settings including the hardware ID and the firmware revision

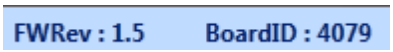


Figure 7: ML4079D Firmware revision

The displayed information is updated whenever any of the fields is being updated.

9.4 BERT Tab

At first glance, after connecting to the board, the user will be able to detect on the GUI the: IP, Serial number, monitoring temperature, channels TX and RX lock, selected bit rate and all the clock configurations...

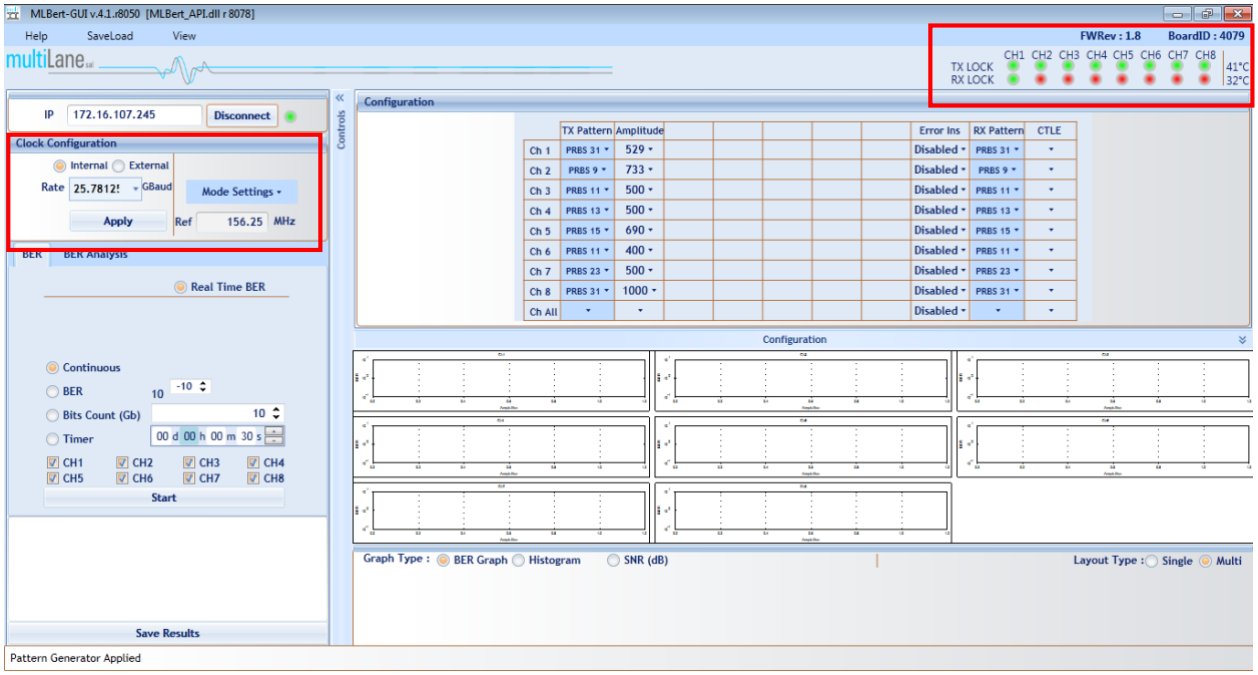


Figure 8: Main features detected after connecting

The user can select and control all the BERT settings.

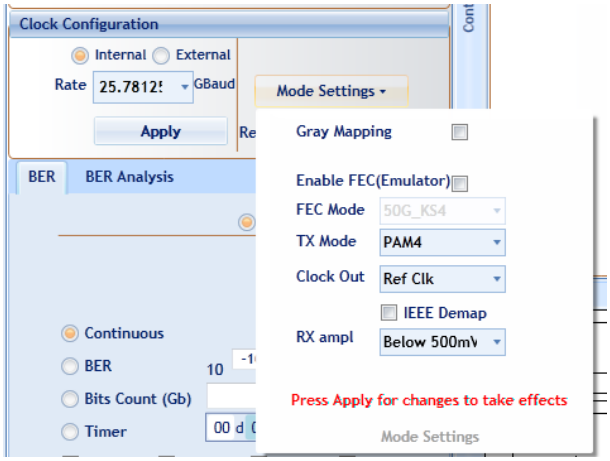


Figure 9: Rate and clock configurations

The ML4079D supports in low rates NRZ mode and in high rate both eye modes: NRZ and PAM4.

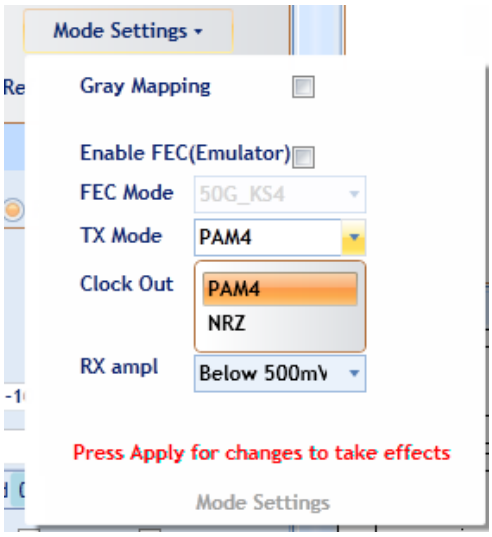


Figure 10: Supported eye modes

To switch between NRZ and PAM4 coding, use the TX Mode setting, then click Apply.
The options Gray Mapping and FEC emulator are only available in PAM4 mode. Gray Mapping enables use of PRBSxxQ defined in IEEE802.3bs. When Gray mapping is enabled, the PRBS13 and PRBS31 under the pattern select menu turn into PRBS13Q and PRBS31Q respectively.

For the clock source, the user can switch between clock-in and clock-out. Whenever any of the clock settings is changed the user should press apply.

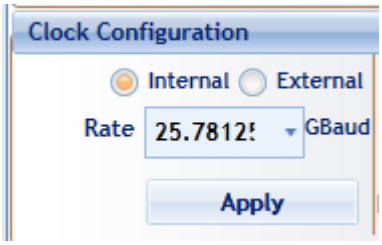


Figure 11: Clock options

If he selects external, which means that he is providing an external clock to the BERT, then he has to make sure the External clock is selected in the clock configuration **and** in the Mode Settings. Then the user should press Apply and provide the appropriate clock input so the RX side of the BERT will be able to lock.

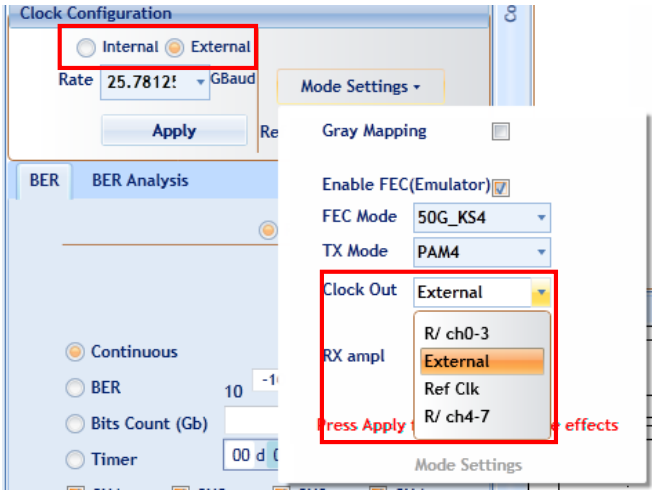


Figure 12: How to select external clock

For the clock-out available options, he has to first select internal. Then he can select reference clock or monitor clock. For optimal results the Ref Clk should be selected.

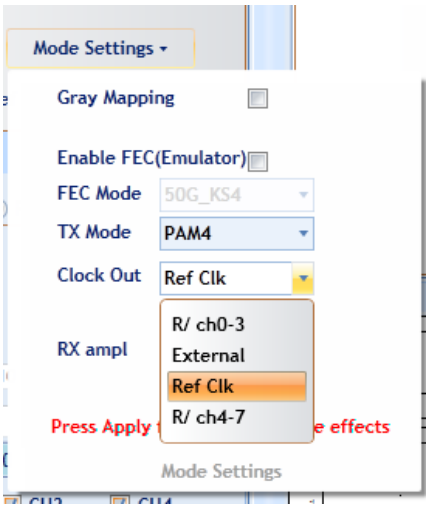


Figure 13: Internal Clock Selection

For the monitor clock he can control the output based on the selected clock divider. And select R/ ch 0-3 if he is using the first four channels or R/ ch4-7 for the last four channels.

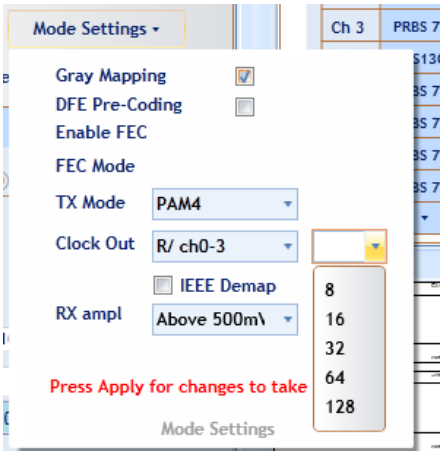


Figure 14: Monitor Clock-out options and dividers

For the BER Test, in the Mode settings Tab the user should choose between two options for the RX amplitude: below or above 500 mV, based on the amplitude he is providing.

This selection will ensure getting more accurate results especially for the BER test. Choosing the option above 500mV lets the BERT lock and run error free at high amplitudes with the optimal settings.

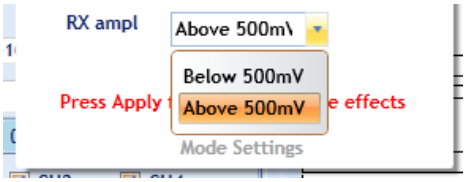


Figure 15: RX amplitude selection

The user can enable KR4, KP4 or KS4 FEC emulator, and he will be able to detect the BER value with and without the FEC emulator correction. The BER graph shows the BER value without FEC.

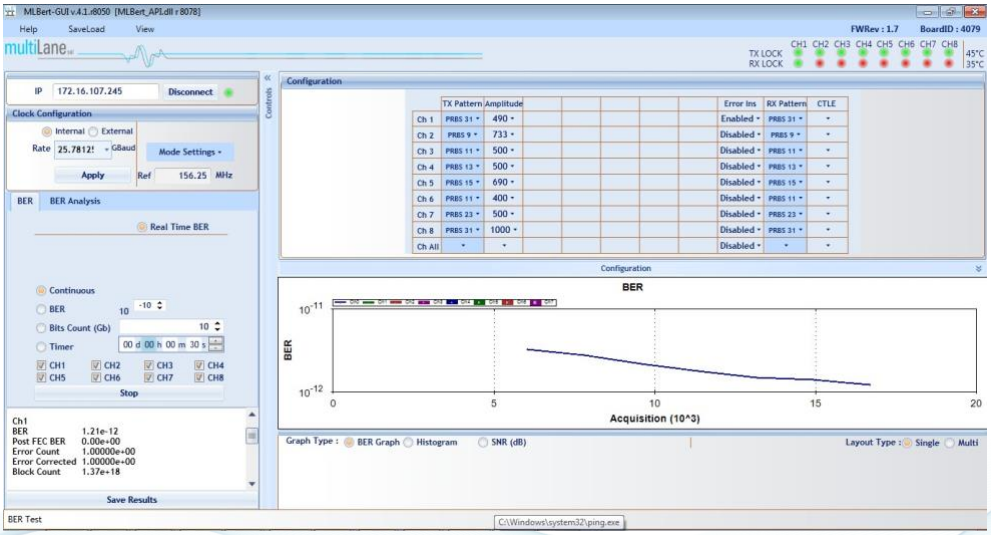


Figure 16: BER with FEC emulator enabled

For the line rate, the user can select any of the listed rates or he can enter any rate he wants, but this rate should be in the supported range as described in table 2.
The user can control all the BERT configurations, channel by channel.

He can choose to run this test in the optimal settings mode: using 70% calibrated settings or 80% calibrated settings, or in advanced mode.

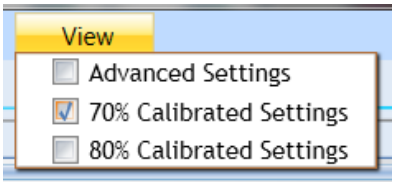


Figure 17: Selecting Advanced or Calibrated Settings mode

In 70% or 80% calibrated settings mode, the optimal settings saved during the calibration process are being applied. And the user will be only able to control and change the amplitude. Based on the selected amplitude the software will automatically calculate the optimal settings.

Configuration

	TX Pattern	Amplitude	Pre Emp	MainTap	Post Emp	InnerAmp	OuterAmp	Error Ins	RX Pattern	CTLE
Ch 1	PRBS13Q	450						Disabled	PRBS13Q	
Ch 2	PRBS 7	90						Disabled	PRBS31Q	
Ch 3	PRBS 7	90						Disabled	PRBS31Q	
Ch 4	PRBS13Q	830						Disabled	PRBS13Q	
Ch 5	PRBS 7	90						Disabled	PRBS31Q	
Ch 6	PRBS 7	90						Disabled	PRBS31Q	
Ch 7	PRBS 7	90						Disabled	PRBS31Q	
Ch 8	PRBS 7	90						Disabled	PRBS31Q	
Ch All								Disabled		

Figure 18: BERT side in optimal settings mode

The ML4079D can output a wide range of pre-defined patterns. In addition to the PRBS patterns, there are linearity and jitter test patterns. Also, on top of the pre-defined patterns the user has the possibility of defining his own pattern.

Note: error detection only works on the PRBS patterns existing in the RX pattern drop down list. It is not possible to do error detection on custom defined patterns.

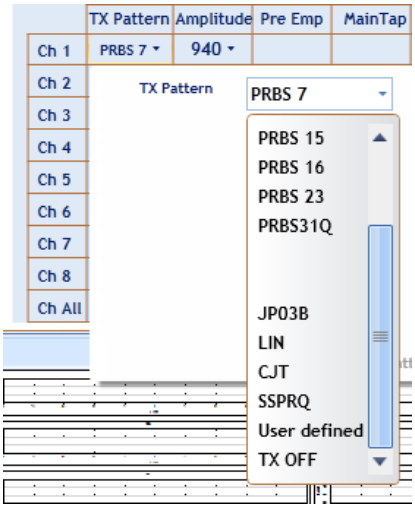


Figure 19: Pattern Selection

In NRZ mode, for each level the corresponding eye amplitude is detected on the scope.

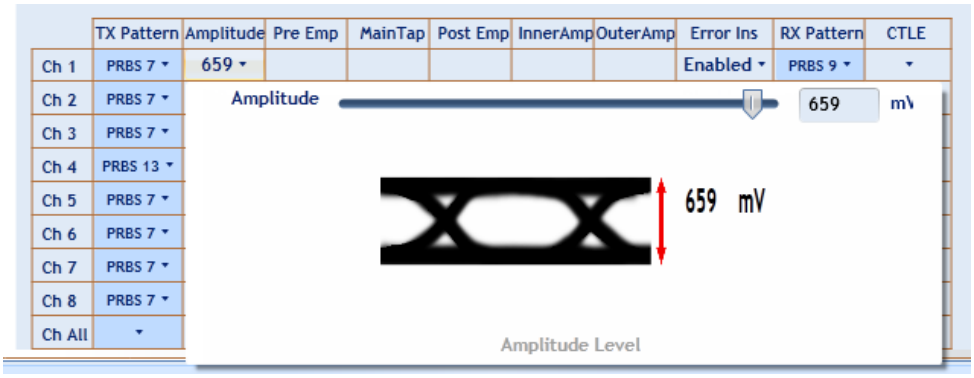


Figure 20: Amplitude control in NRZ mode and with the optimal settings applied

In PAM4 mode, for each level the corresponding total eye amplitude is detected on the scope, this value is equal to the sum of the inner eye amplitude and two outer eye amplitudes. As shown in figure 19.

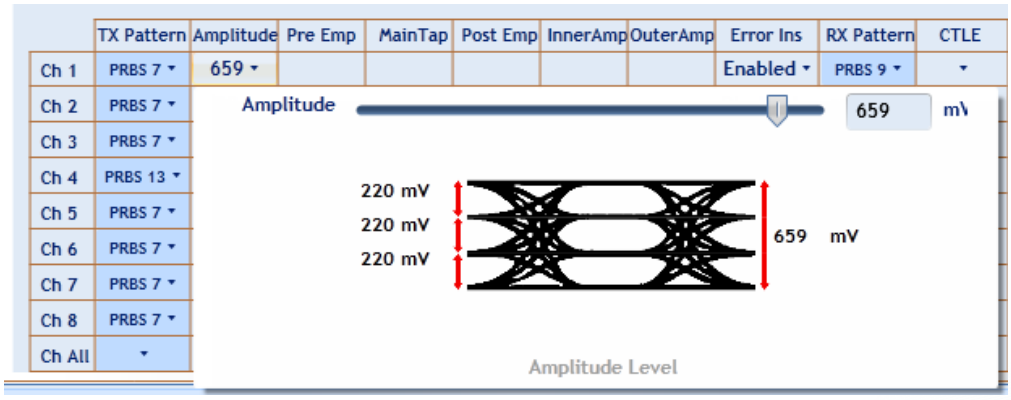
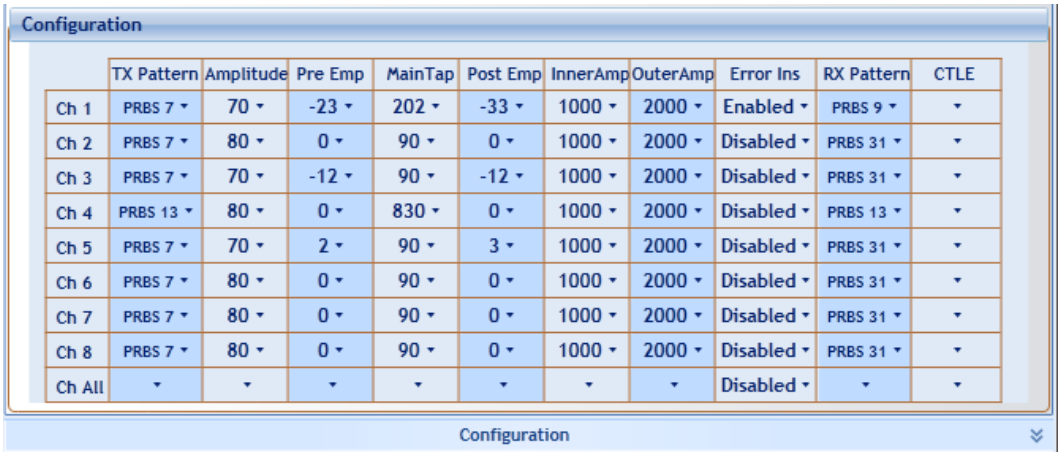


Figure 21: Amplitude control in PAM4 mode and with the optimal settings applied

If the customer desires to control all the parameters, then he needs to go the advanced mode While switching between advanced settings and calibrated settings modes the user will be modified that the optimal settings are being applied.

Figure 22: Settings being applied

If Advanced settings mode is selected then the BERT configuration window will be displayed as follows and the user will have access to control the amplitude and the FFE taps:



	TX Pattern	Amplitude	Pre Emp	MainTap	Post Emp	InnerAmp	OuterAmp	Error Ins	RX Pattern	CTLE
Ch 1	PRBS 7	70	-23	202	-33	1000	2000	Enabled	PRBS 9	
Ch 2	PRBS 7	80	0	90	0	1000	2000	Disabled	PRBS 31	
Ch 3	PRBS 7	70	-12	90	-12	1000	2000	Disabled	PRBS 31	
Ch 4	PRBS 13	80	0	830	0	1000	2000	Disabled	PRBS 13	
Ch 5	PRBS 7	70	2	90	3	1000	2000	Disabled	PRBS 31	
Ch 6	PRBS 7	80	0	90	0	1000	2000	Disabled	PRBS 31	
Ch 7	PRBS 7	80	0	90	0	1000	2000	Disabled	PRBS 31	
Ch 8	PRBS 7	80	0	90	0	1000	2000	Disabled	PRBS 31	
Ch All								Disabled		

Figure 23: BERT Configurations in PAM4 and Advanced Mode with 3 taps option

Main-Tap, Pre and Post Emphasis level varies between ±1000. The amplitude slider does not show anymore the values that have been saved during the calibration. The user can go up to 120% and the corresponding amplitude is detected on a scope.

To access the 7 taps FIR the user should select the Advanced settings then go to the mode settings tab and enable the 7 taps option, and press apply.

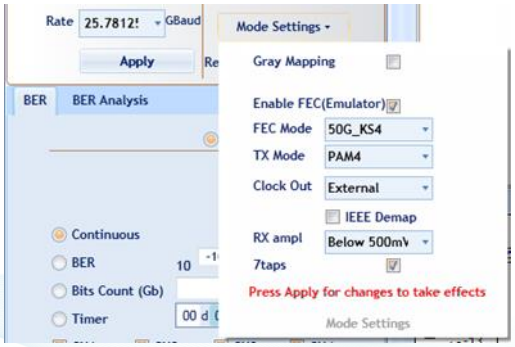


Figure 24: Enabling the 7 taps FIR option

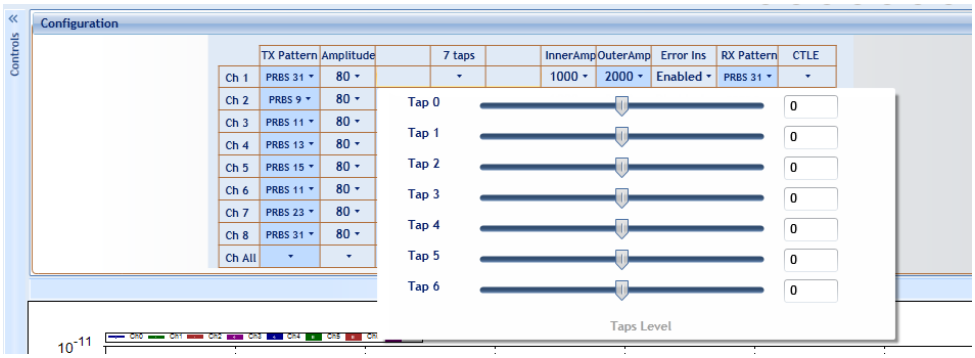


Figure 25: Configurations Tab in PAM4 and Advanced Mode with 7 taps option

The user can test the BER, histogram and SNR, on the selected channels.

Error insertion and CTLE can be controlled channel by channel.

All these measurements can be performed on all the rates, patterns and in NRZ and PAM4 mode.

Below are shown some screenshots showing the eye in PAM4 and NRZ modes using to the MLDSO. These screenshots are captured, with the 80% calibrated settings being applied.

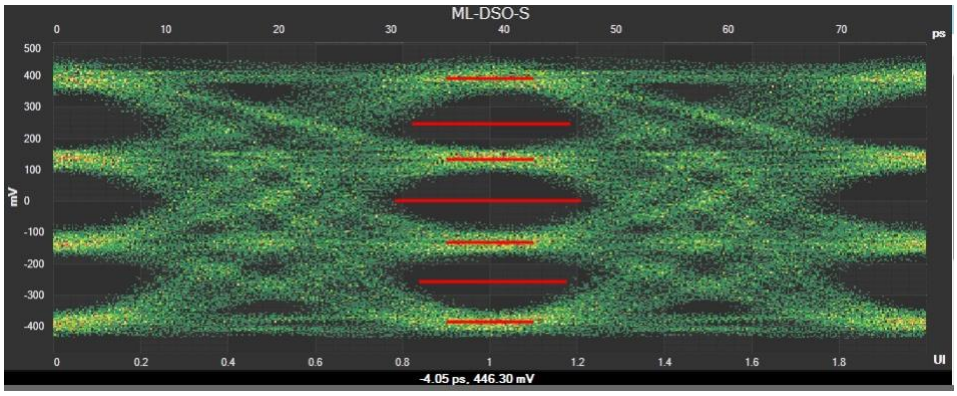


Figure 26: PAM4 mode, high rate

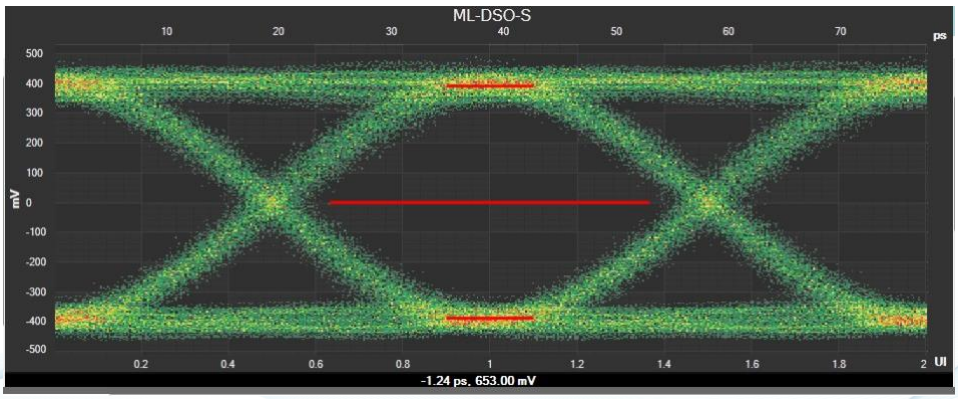


Figure 27: NRZ mode, high rate

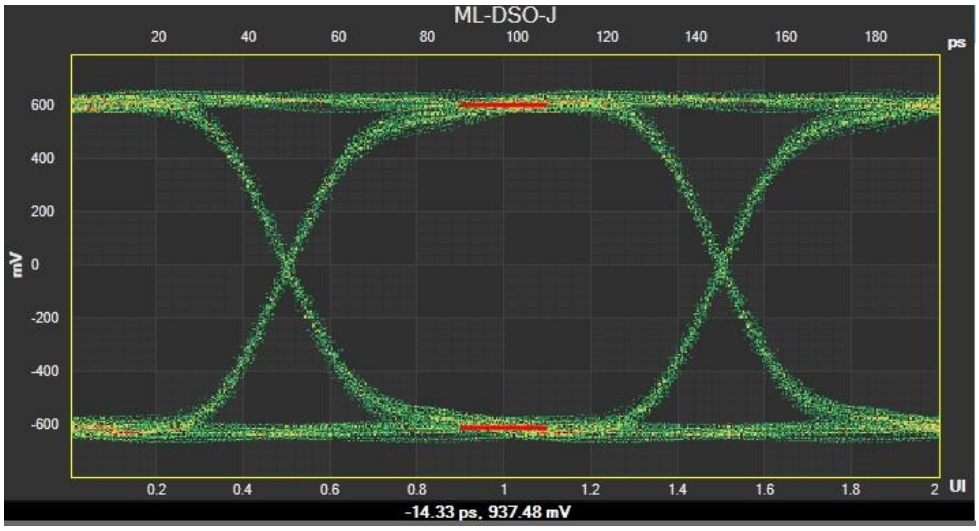


Figure 28: NRZ mode, low rate

Figure 29 shows the 7 taps settings that are used to capture figure 30(NRZ eye) and 31 (PAM4 eye).

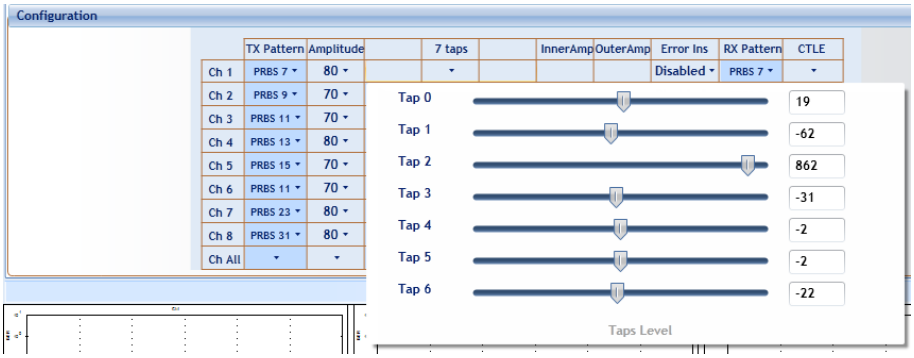


Figure 29: 7 taps values

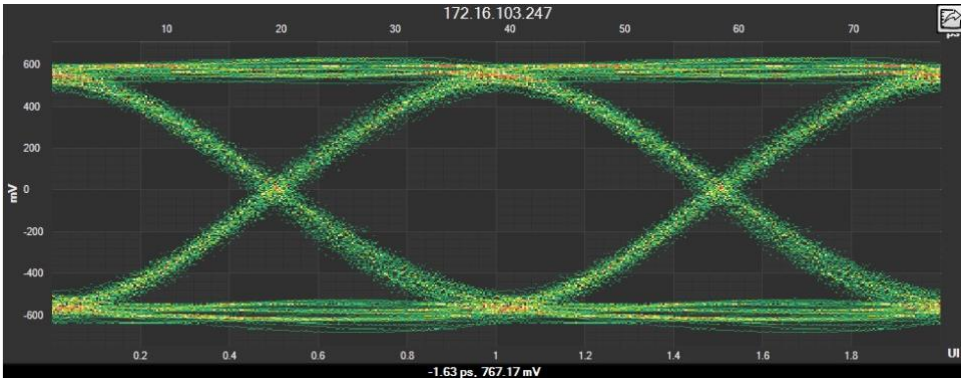


Figure 30: Captured eye in NRZ mode using 7 taps settings

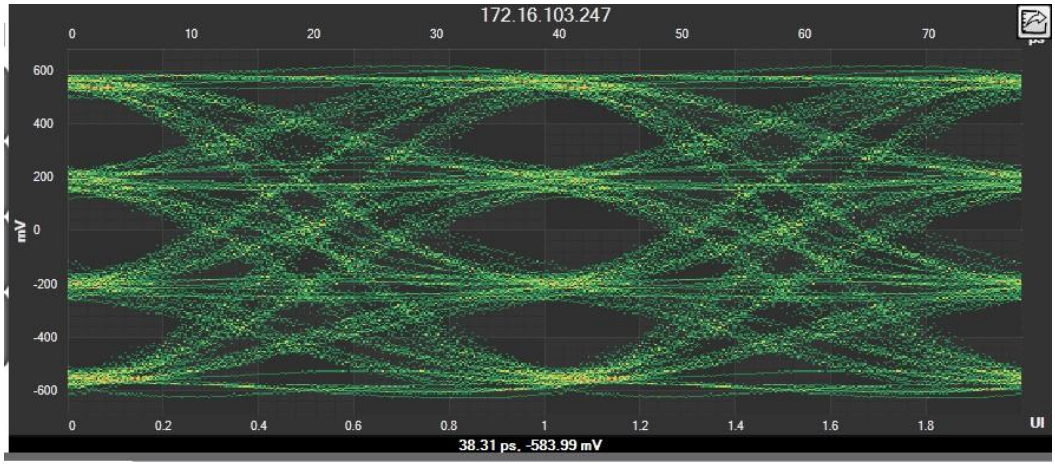


Figure 31: Captured eye in PAM4 mode using 7 taps settings

9.5. BERT Measurements

To be able to start BER measurements, the instrument ports should be in the loopback mode, which means the TX ports should be connected to the RX ports and the PPG and ED patterns should match. It is not necessarily to supply a PRBS from the same physical instrument – the source can be a different instrument and the error-detector of the ML4079D can derive its own clock from the received data (no need for a separate clock link). However, if Gray coding is used in the source, one should tell the receiver to expect Gray coding as well. There should be a match in pattern, polarity and coding to have lock. If an external clock source is used then the clock value should be equal to the value of the reference clock.

The user can run the BER test on selected channels continuously, or choose a target BER or set a timer.

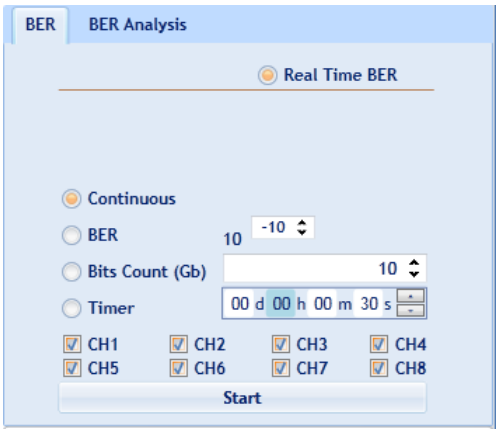


Figure 32: BER control panel

The BER values are displayed per channel and their corresponding BER graph. In PAM4 the value of the BER at MSB and LSB is shown. The graph shows the total BER value.

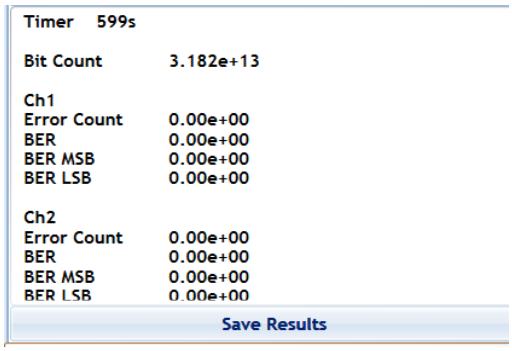


Figure 33: BER values in NRZ mode

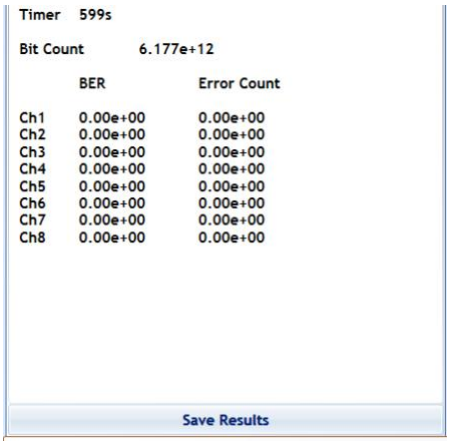


Figure 34: BER values in PAM4 mode

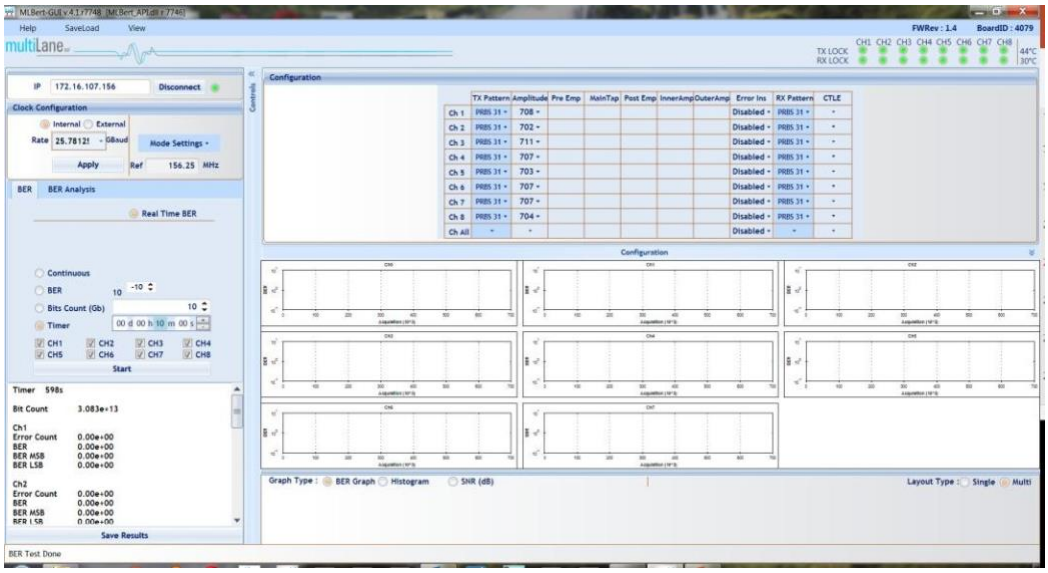


Figure 35: BER test on 8 channels

The user can test the BER, histogram and SNR, on the selected channel, in NRZ and PAM4 modes.

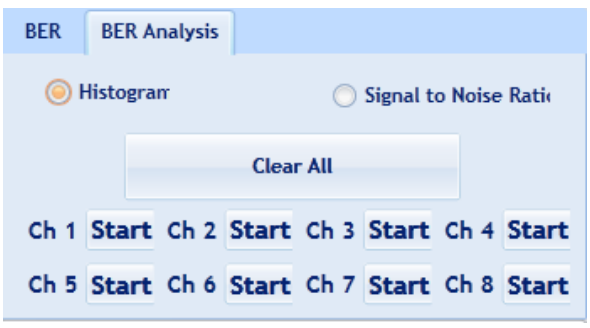


Figure 36: BER analysis tab

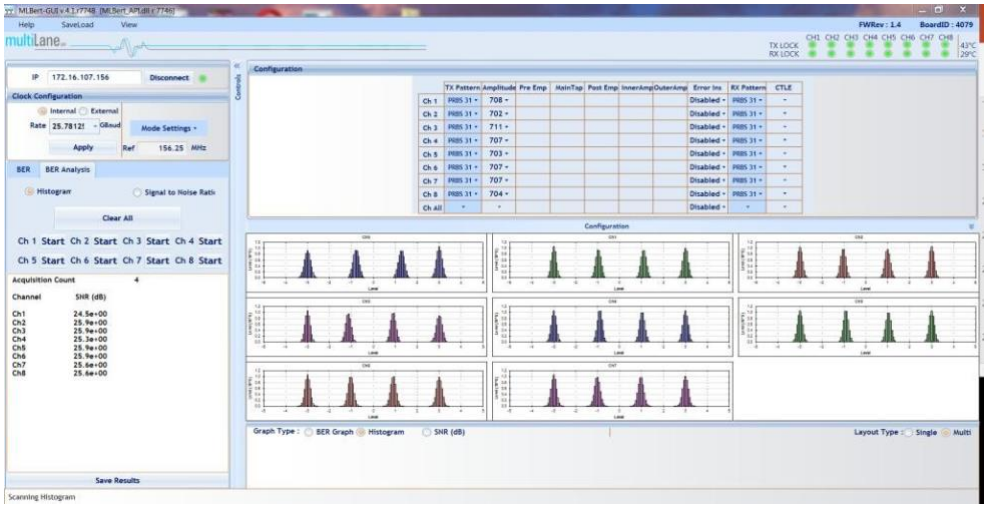


Figure 37: Histograms in PAM4 mode

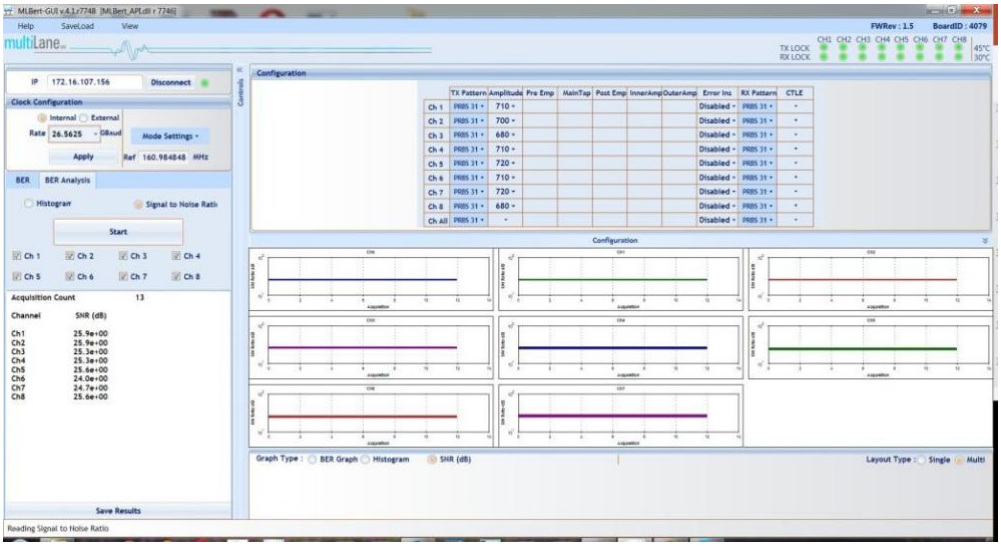


Figure 38: SNR in PAM4 mode

This BERT gives the user the possibility to insert errors by enabling the error insertion option.

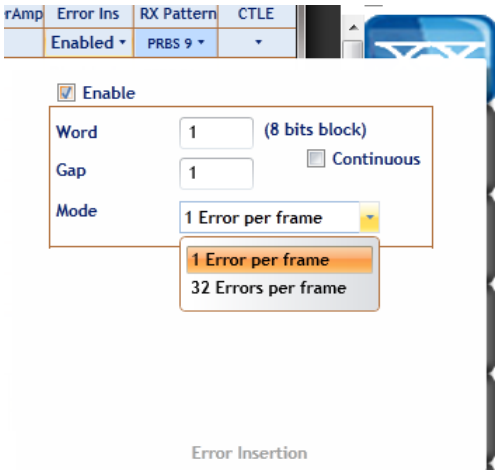


Figure 39: Error Insertion options in NRZ mode

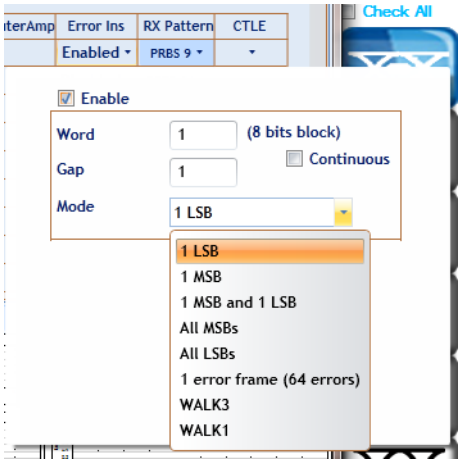


Figure 40: Error Insertion options in PAM4 mode

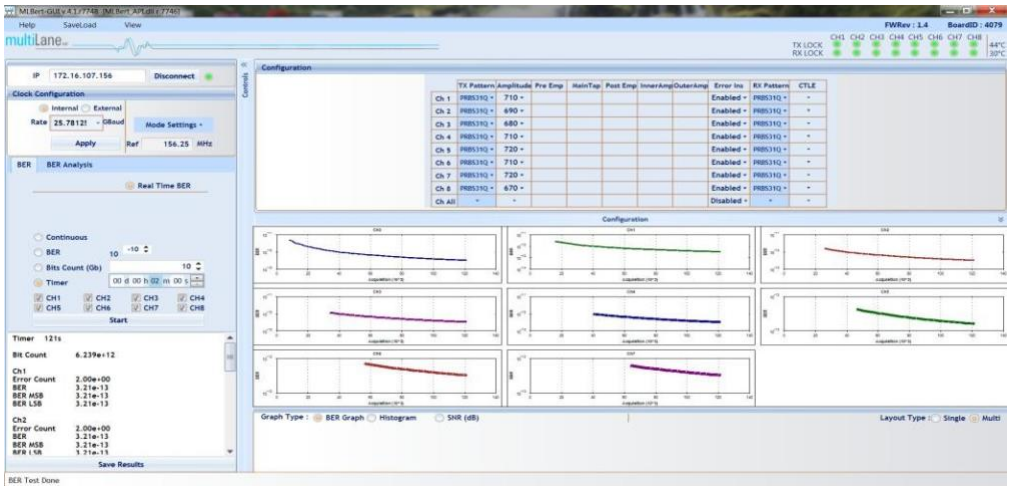


Figure 41: BER measurement with 1 error inserted at the MSB and 1 error at the LSB

At the receiver's side, CTLE can be added. The user can choose between the two CTLE options. The CTLE slider supports up to 64 steps. It can be tuned on a range of around 8 dB

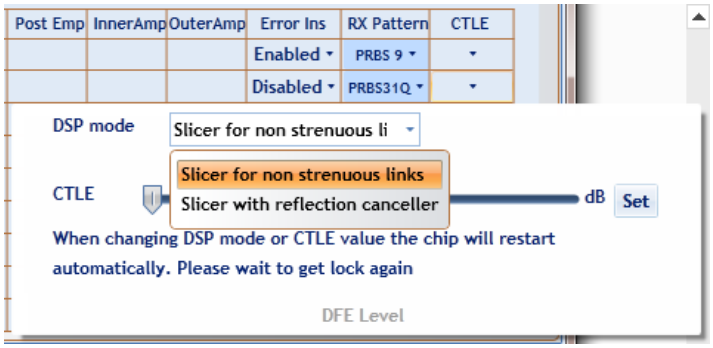


Figure 42: CTLE options

10. IP Changer Tool

If the user needs to change the IP of the board, he can access the below link, where he can find all needed tools (software and user guide).

Figure 43: IP changer GUI and User Guide

Figure 44: Ethernet Configuration Software

11. Revision History

Revision number	Date	Description
1.0	1-4-2019	Document created
1.1	2-18-2019	• 7 taps FIR description and added in paragraph 7 and 11.4 • FEC emulator description added to paragraph 8 • Screenshots related to the 7 tap feature added to the user manual section